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Search History

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L2	programmable adj1 element	1418	L2
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L11: Entry 4 of 13 File: USPT May 22, 2001

DOCUMENT-IDENTIFIER: US 6236219 B1
**** See image for Certificate of Correction ****
TITLE: Programmable voltage divider and method for testing the impedance of a programmable element

Parent Case Text (2):
The following pending U.S. patent applications entitled: "An Efficient Method of Determining Acceptable Resistance of a Blown Fuse," Ser. No. 08/813,525, filed Mar. 7, 1997, and "Method and Apparatus for Checking the Resistance of Antifuses," Ser. No. 08/813,767, filed Mar. 7, 1997, issued Nov. 9, 1999 as U.S. Pat. No. 5,982,656 are related to the present application.

Brief Summary Text (2):
The present invention relates generally to electronic circuits, and more specifically to a programmable circuit that allows one to test the impedance of a programmable element, such as a fuse, during a test mode, and to a method for performing such a test.

Brief Summary Text (5):
These integrated circuits each typically include a bank of nonvolatile, programmable memory elements that the manufacturer programs to set a circuit in the desired operational mode or circuit configuration. Examples of such elements include electrically erasable and programmable read-only memory (EEPROM) cells, fuses, and antifuses. An integrated circuit often incorporates into its programmable bank the type of programmable element that is the most similar to other elements or components of the circuit. For example, a Flash-EEPROM device often includes a bank of EEPROM cells, but a dynamic random access memory (DRAM) often includes a bank of antifuses, which are similar in structure to the DRAM storage capacitors. Furthermore, such a programmable element typically has a first impedance in an unprogrammed state, and a second, different impedance in a programmed state. For example, an antifuse has a high impedance in an unprogrammed state, and thus is essentially an open circuit, and has a low impedance in a programmed state, and thus is essentially a short circuit. Conversely, a fuse is essentially a short circuit in an unprogrammed state, and is essentially an open circuit in a programmed state.

Brief Summary Text (7):
A problem with this analog testing technique is that it often takes too long for high-density integrated circuits. As the number of circuit components in an integrated circuit increases, so does the number of operational modes and circuit configurations that the circuit supports. Therefore, the number of programmable elements in the programmable bank also increases to accommodate the additional operational modes and circuit configurations. For example, a 4 megabit DRAM may have 20 antifuses in its programmable bank, but a 64 megabit DRAM may have 640 antifuses. Furthermore, measuring the impedance in an analog fashion is relatively slow because of the parasitic capacitances associated with the test path and each programmed element. Thus, increasing the storage capacity of a DRAM by a factor of 16 can potentially increase the number of antifuses, and thus the already lengthy testing time, by a factor of 32. Additionally, testers that can perform analog measurements are often expensive and complicated to operate in the analog-testing

mode.

Brief Summary Text (13):
An advantage of the present invention is that it allows faster testing of programmable elements as compared with the prior art. Another advantage is that the present invention allows digital testing of programmable elements instead of analog testing.

Drawing Description Text (7):
FIG. 6 is a schematic diagram of an alternative embodiment of the programmable elements of FIGS. 1, 2 and 5.

Detailed Description Text (3):
The programmable circuit 12.sub.0 includes a programmable element 18.sub.0, which is an antifuse in this first embodiment of the invention. A first node of the antifuse 18.sub.0 is coupled to a test node 20, which is common to the first nodes of all the antifuses 18.sub.0 -18.sub.n. A second node is coupled to an isolation device 19.sub.0, which limits the voltage across the antifuse 18.sub.0 during normal operation of the bank 10. In one aspect of the invention, the device 19 is an NMOS transistor, which has its gate coupled to a voltage V.sub.1 during normal operation of the bank 10, and to 0 V, i.e., ground, during programming of the bank 10.

Detailed Description Text (19):
FIG. 5 is a schematic diagram of a programmable bank 54 according to a third embodiment of the invention. The bank 54 is similar to the bank 10 of FIG. 1 and the bank 46 of FIG. 2, except that programmable circuits 59.sub.0 include programmable elements 56.sub.0 -56.sub.n, and a test circuit 55 includes a voltage source 58, which generates a negative voltage -VT on the common node 20 during the digital test mode. In one aspect of the invention, the elements 56.sub.0 -56.sub.n are either laser-cutable fuses or electrically programmable fuses. Thus, unlike the antifuses 18.sub.0 -18.sub.n of FIGS. 1 and 2, the fuses 56.sub.0 -56.sub.n have a low impedance when unprogrammed, and have a high impedance when programmed. Because the fuses 56.sub.0 -56.sub.n are not antifuses, the programming circuitry 32 and the isolation transistors 19 of the banks 10 and 46 may be omitted. In this case, the fuses 56.sub.0 -56.sub.n are programmed using conventional means (not shown in FIG. 5) that are external to the device that incorporates the bank 54. Alternatively, if the fuses 56.sub.0 -56.sub.n are electrical fuses, then the bank 54 may include circuitry that is similar to the programming circuitry 32 of FIGS. 1 and 2. But for clarity, FIG. 5 includes no programming circuitry. Because the circuit 59.sub.0 is similar in structure and operation to the circuits 59.sub.1 - 59.sub.n, the operation of the bank 54 is discussed below in greater detail with reference to the circuit 59.sub.0 for clarity.

Detailed Description Text (26):
FIG. 6 is a schematic diagram of nonvolatile programmable element 60 according to an alternative embodiment of the invention. The programmable element 60 is a EEPROM cell that includes a floating gate 62. In a conventionally defined unprogrammed state, there is no voltage stored on the floating gate 62, and thus the EEPROM cell 60 has a low impedance, i.e., acts as a closed circuit, when a voltage is applied to its gate. In a conventionally defined programmed state, a negative voltage is stored on the floating gate 62, and thus the EEPROM cell 60 has a high impedance, i.e., acts as an open circuit, when a voltage is applied to its gate. Thus, the EEPROM cell 60 is similar to the fuse elements 56.sub.0 -56.sub.n of FIG. 5, and in one aspect of the invention may be used in place of these fuse elements in the bank 54.

Detailed Description Text (31):
During the conventional test mode, the circuit 72 generates a test voltage, and external test circuitry measures the current flowing through the circuit 66 under

test to determine the resistance of the programmable element therein and whether or not it has a desired value.

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L11: Entry 11 of 13 File: USPT Nov 22, 1994

DOCUMENT-IDENTIFIER: US 5367207 A
** See image for Certificate of Correction **
TITLE: Structure and method for programming antifuses in an integrated circuit array

Abstract Text (1):
This invention provides a structure and method for interconnecting logic devices through line segments which can be joined by programming antifuses. One of several programming lines can be connected through an interconnect line segment to each terminal of each antifuse in the array. Interconnect line segments connected to opposite terminals of the same antifuse are connected to a different programming line in order to be able to apply different voltages to the two terminals of the antifuse. An addressing structure selectively connects interconnect line segments to their respective programming lines, and programming voltages applied to the programming lines cause a selected antifuse to be programmed. A novel addressing feature sequentially addresses two transistors for the line segments to be connected, and takes advantage of a capacitive pumped decoder to maintain the addressed transistors turned on while programming voltages are applied. The structure also allows for testing of logic devices by applying test voltages to the programming voltage lines and/or sensing logic device output on programming voltage lines. The structure and method also permit measuring resistance of the programmed antifuses. No separate testing overhead structure is needed.

Brief Summary Text (13):
Further structures and methods for programming antifuses are known. Elgamal et al., in U.S. Pat. No. 4,758,745 describes a structure and method for programming antifuses which, as shown in FIG. 4 (Elgamal FIG. 1B), uses one channel control logic unit 23 for controlling the voltage to be applied to each line in an array. As shown in FIG. 5, (Elgamal FIG. 5, which is described in Elgamal col. 8, starting at line 53), pass transistors 40 are provided in parallel with programmable elements (antifuses) 46. Pass transistors 40 are used as feed through transistors during programming of one of the programmable elements 46. By turning on all transistors in a horizontal channel except the transistor for which an antifuse is to be programmed, a programming voltage can be applied to that antifuse. For example by turning on all transistors in channel 62c except transistor 40, and applying low and high voltages to opposite ends of the channel 62c, it is possible to generate enough voltage across terminals of antifuse 46 to program antifuse 46. Because the programming voltage must be applied through a series of transistors such as transistor 40, the programming current for programming antifuse 46 will be limited by the resistance of the transistors in channel 62c through which the current must flow. Since final resistance of the programmed antifuse depends upon current during programming, the final antifuse resistance is also limited by the resistance of transistors in channel 62c. Further, the arrangement of FIG. 5 is not easily scaled. Since the resistance of a channel such as 62c depends upon the number of transistors in series, if one were to design a set of devices using the principles of FIG. 5, it would be necessary to use different design rules for each device having a different number of transistors in series. If decoders were added midway when scaling to a larger device, so that a programming current was applied through only a set number of transistors in series, the efficiency of having decoding performed entirely at the periphery of the chip would be lost.

Detailed Description Text (49):
When programming is complete, the programming voltage is removed from the programming bus, and addressing voltages are removed from the second pair of address lines. Completion of programming may be established by a set time interval, by achieving an established programming current, or by removing the programming voltage and applying a voltage for measuring on-resistance (discussed earlier).

CLAIMS:

18. A structure for measuring resistance in a programmed antifuse in an array of antifuses in an integrated circuit structure comprising:

a set of programming voltage lines to which programming voltage can be applied;

a plurality of antifuses;

for each antifuse a first programming voltage transistor for programmably connecting a first terminal of said antifuse to a first one of said programming voltage lines, and a second programming voltage transistor for programmably connecting a second terminal of said antifuse to a second one of said programming voltage lines;

at least one pair of measurement transistors connected in series between two of said programming voltage lines, said measurement transistors being manufactured to have the same resistance characteristics as said programming transistors;

whereby resistance of said measurement transistors can be measured and used as a reliable estimate of resistance of said programming transistors.

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L11: Entry 13 of 13 File: USPT Oct 6, 1987

DOCUMENT-IDENTIFIER: US 4698589 A
TITLE: Test circuitry for testing fuse link programmable memory devices

Brief Summary Text (2):
The present invention relates generally to testing circuitry, and more specifically to testing circuitry for measuring the resistance of programmable elements in fuse link memory devices.

Brief Summary Text (11):
The testing circuit may include a multiplexing switching means connected between the plurality of fuses and the sensing amplifier for multiplexing the programmable elements having these fuses with a single sensing amplifier. In the above preferred embodiments, the switching gate means includes an N-channel device having its source connected to the fuse of the programmable element and its drain connected to the input of the sensing amplifier. The gate of the switching gate means would thereby be triggered by multiplexing signals.

CLAIMS:

1. A testing circuit for determining the proper functioning of a programmable element in a memory device having a sensing means connected to said programmable element for providing a first signal when a current flowing through said programmable element is below a specified threshold and a second signal when said current flow is above said specified threshold, said testing circuit comprising:

a variable resistance means forming a voltage divider with said programmable element, said sensing means being connected at a nodal point therebetween, said variable resistance means providing a first resistance during a normal read operation of said memory device and a second resistance during a testing operation of said memory device for varying said current flow, whereby current flowing through said programmable element is sensed during said operations by said sensing means.

4. The testing circuit of claim 2, wherein said second resistance is less than said first resistance for testing whether said programmable element is properly intact.

5. The testing circuit of claim 2, wherein said second resistance is greater than said first resistance for testing whether said programmable element has been properly programmed.

6. The testing circuit of claim 3, further comprising a plurality of multiplexing switching means and a plurality of programmable elements, wherein each of said multiplexing switching means is connected between each of said programmable elements and said sensing means for multiplexing said plurality of programmable elements with said sensing means.

7. The testing circuit of claim 6, wherein each of said multiplexing switching means includes an N-channel insulated gate field effect device having its source

connected to one of said programmable elements, its drain connected to said input means of said sensing means and to said variable resistance means, and its gate connected to a source of multiplexing signals.

8. A testing circuit for measuring the resistance of a programmable element in a memory device, comprising:

a variable resistance means connected to said programmable element for providing a first resistance during a read operation of said programmable element and at least one other resistance during a testing operation of the same, thereby varying a current flow through said programmable element respectively; and

a sensing means connected at a nodal point between said programmable element and said variable resistance means for sensing said current flow, thereby sensing said resistance of said programmable element.

13. The testing circuit of claim 8, wherein said sensing circuit includes a sensing amplifier having an input means and an output means for providing a first output signal when a current flowing through said programmable element is below a specified threshold and a second output signal when said current is above said specified threshold.

14. A sensing circuit for sensing a current flowing through a programmable element in a memory device, said sensing circuit comprising:

a sensing means having an input means connected to said programmable element for providing a first signal when said current flowing through said programmable element is below a specified threshold and a second signal when said current flowing through said programmable element is above a certain threshold; and

a varying current level means connected to an output of said programmable element and said input means of said sensing means for providing a first current level during a normal read operation of said memory device and a second current level during a testing operation of said memory device.

15. The sensing circuit of claim 14, wherein said varying current level means includes a current mirror having an output stage connected to said programmable elements and an input stage for varying the current flow in said output stage in response to a plurality of logic input signals provided at the input stage.

17. The sensing circuit of claim 16, wherein said output stage of said varying current level means includes a single N-channel insulated gate field effect transistor connected to said programmable element and wherein said parallel connected control legs include a plurality of N-channel insulated gate field effect transistors having respective input stages for receiving said logic input signals, whereby said logic input signals determined the number of N-channel transistors which are active in the input stage of said current mirror during said normal and testing operations.

19. The sensing circuit of claim 18, further comprising a plurality of multiplexing switching means and a plurality of programmable elements, wherein each of said multiplexing switching means is connected between each of said programmable elements and both said sensing means and varying current level means for multiplexing said plurality of programmable elements with said sensing means and varying current level means.

20. The sensing circuit of claim 19, wherein each of said multiplexing switching means includes an N-channel insulated gate field effect device having its source connected to one of said programmable elements, its drain connected to both said input means of said sensing means and to varying current level means, and its gate

connected to a source of multiplexing signals.

21. The sensing circuit of claim 14, wherein said means for varying current level includes a variable resistance means forming a voltage divider with said programmable element, said sensing means being connected at a nodal point therebetween, said resistance means providing a first resistance during a normal read operation of said memory device and a second resistance during a testing operation of said memory device for varying said current flow, whereby current flowing through said programmable element is sensed during said operations by said sensing means.

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